A combination of multi-edge coding and independent coding lines for time-to-digital conversion

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Abstract—The paper describes a new method for time-to-digital conversion that allows achieving the conversion resolution far below the propagation time of the fastest delay buffer in integrated circuit (IC). The method is a combination of the multi-edge time coding and time digitization in independent coding lines. The implementation of such combination and assessment of its effectiveness are the main aims of this research. The article also describes the main design issues that were solved during the implementation of method in an FPGA device. They include: the generation of a pattern square signal with a certain amount of edges and possibly minimal delays between them, the elimination of bubble errors and reduction of internal interferences in IC.

Keywords — time-to-digital conversion; multi-edge coding; independent coding lines; time counter

I. INTRODUCTION

The fast development of technology causes the necessity of creation of still more and more accurate and faster measurement techniques. This problem also applies to precise time metrology, which is crucial in laser rangefinders, navigation systems, nuclear physics researches, universal laboratory equipment and others. Methods of time interval measurements are generally divided into two main groups; i.e., analog and digital [1]. The second group of methods has become more popular recently due to easiness of implementation in ICs. Among methods in this group two of them are dominating; i.e., the method of pulse shrinking (or stretching) and direct conversion method. In the former one an achievement of high resolution and wide measurement range is possible by extension of chain of pulse-shrinking elements or by application of cyclic pulse shrinking [2,3]. The chain extension is associated with an increase in the linearity error of conversion, whereas cyclic pulse shrinking causes an accumulation of jitter of edges of a measured pulse circulating in the loop.

The direct conversion method is based on the use of tapped delay line. The most often implementation of such delay line involves a chain of delay buffers and associated D flip-flops (fig. 1a). In this text such implementation of delay line is called time coding delay line (TCDL). The measured time interval is defined by the rising edges of pulses START and STOP. The rising edge of the START pulse propagates through consecutive buffers (multiplexers in our design) of the line. Each buffer has the propagation delay of \( \tau_i \). When the rising edge of the STOP pulse appears, flip-flops store the current state of TCDL (fig. 1b). The value of measured time interval is calculated as a sum of propagation delays of all buffers that were travelled through by the START pulse until the STOP pulse appeared. In the ideal case, when the delays of buffers are identical, this value can be calculated as \( T_m = k \times \tau \), where \( k \) is the number of the last flip-flip storing the high state (1).

To improve the main parameters of conversion more advanced processing method can be used, for example method based on the independent coding lines [4] or multi-edge coding (also called wave union) [5]. In the first of them the measurement of time interval is performed simultaneously in several TCDLs that create the virtual equivalent coding line (ECL). The result of measurement is calculated as a result of conversion in ECL. The main disadvantage of this method is the need to implement a large number of lines in order to achieve high resolution of conversion. The second method allows for obtaining the resolution lower than the propagation time of a single delay cell, without the need to multiply the TCDLs. This is accomplished by coding not a single, but several edges of signal START containing information about the measured time interval. However, each additional edge causes the necessity of extension of the TCDL. A long coding line in turn is sensitive to changes in ambient temperature and power supply. Therefore, this line should be as short as possible. The effective solution of this problem is a combination of the independent coding lines and multi-edge coding methods. In this novel method, a multi-edge START signal propagates through several TCDLs at the same time. After the occurrence of the STOP signal, the numbers of flip-flops that saved the brink states (0-1 or 1-0) are searched. The sum of numbers found determines the quantization step in
resulting ECL (fig. 2). Its width is evaluated during a calibration process performed with the use of statistical code density test (SCDT) [6].

Fig. 2. Principle of ECL creation in the proposed method.

The next analysed issue was the bubble errors that occur in the output code of the TCDLs [7]. They are mainly caused by the influence of temperature drift and supply noise on internal propagation delays in IC. In the TDC with a single-edge coding, these errors can be eliminated by virtual rearrangement of cells in TCDL. However, in the multi-edge coding method all edges of the pattern signal are coded and such approach is not efficient enough. To eliminate the bubble errors an additional circuit has been developed that detects excess logic transitions in the output word of coding line and corrects them.

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During the first test of the designed TDC the optimal number of edges and the number of TCDLS have been evaluated. The highest resolution of converter (0.92 ps) was obtained with the use of 6-edge pattern and three TCDLS (fig. 3).

The highest resolution of converter (0.92 ps) was obtained with the use of 6-edge pattern and three TCDLS (fig. 3). Generation of a pattern signal with greater number of edges than 6 is difficult and it takes a long time, which increases the conversion time of TDC. During tests it also was observed that the falling edge propagates through the TDCL faster than the rising one. The inequality of the times can lead to vanish of pattern pulses. Therefore, to get the further improvement in resolution, the increase in the number of lines is suggested.

Table I compares parameters of the proposed TDC with some prior published works in FPGA technologies. The assessment criteria are resolution, range and linearity errors. It can be concluded that the developed TDC is one of the best solutions implemented in the FPGA devices so far.

Table I. Measurement performance of selected TDCs

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<tbody>
<tr>
<td>[3], 2010</td>
<td>PS/90 FPGA</td>
<td>42</td>
<td>18</td>
<td>0.98</td>
<td>4.17</td>
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<tr>
<td>[8], 2013</td>
<td>WU/65 FPGA</td>
<td>11</td>
<td>&lt;0.500</td>
<td>2.7</td>
<td>9</td>
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<tr>
<td>[9], 2013</td>
<td>MEC/45 FPGA</td>
<td>5.34</td>
<td>0.428</td>
<td>2.93</td>
<td>3.82</td>
</tr>
<tr>
<td>This work</td>
<td>MECICL/45 FPGA</td>
<td>0.9</td>
<td>0.428</td>
<td>2.91</td>
<td>15.7</td>
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